CLAIM AMENDMENTS

Please amend claims 1 and 5 as indicated in the following.

Please cancel claim 4 without prejudice or disclaimer as indicated in the following.

Claims Listing:

1. (Currently Amended) A method comprising:
discharging a plurality of bit lines during an inactive memory access period;
applying a charging pulse on a select one of the plurality of bit lines; and
after applying the charging pulse, waiting a delay time before sensing a voltage difference between the select one of the plurality of bit lines and a reference line, the delay time sufficient to allow the select one of the plurality of bit lines to be pulled towards a voltage level corresponding to a stored value in a selected memory bit cell.

2. (Previously Presented) The method, as recited in Claim 1,wherein the charging pulse has a width and the sensing occurs during a delay after the charging pulse, wherein the width and the delay are determined according to a size of a memory.

3. (Previously Presented) The method, as recited in Claim 1, wherein the charging pulse has a width and the sensing occurs during a delay after the charging pulse, wherein the memory is a compilable memory and the width and the delay are calculatable according to a selectable size of a memory.

4. (Canceled)

5. (Currently Amended) ~~The method, as recited in Claim 1, further comprising:~~ A method comprising:

discharging a plurality of bit lines during an inactive memory access period;

applying a charging pulse on a select one of the plurality of bit lines; and

after applying the charging pulse, waiting a delay time before sensing [[the]]a voltage difference between the select one of the plurality of bit lines and the reference line, the delay time sufficient to allow the reference line to be pulled towards a reference voltage

6. (Previously Presented) The method, as recited in Claim 1, wherein the voltage difference is greater than or equal to 100 millivolts.

7. (Currently Amended) The method, as recited in Claim 1, wherein the voltage difference is greater than or equal to 150 millivolts.

8. (Original) The method, as recited in Claim 1, further comprising:

applying another charging pulse on the reference line.

9. (Original) The method, as recited in Claim 1, further comprising:

discharging the reference line during the inactive memory access period.

10. (Original) The method, as recited in Claim 1, wherein applying the charging pulse on the select one of the plurality of bit lines draws a voltage of the select one of the plurality of bit lines to a midpoint voltage level.

11. (Original) The method, as recited in Claim 1, further comprising:

applying a charging pulse on the reference line, wherein applying the charging pulse on the reference lines draws a voltage of the reference line to a midpoint voltage level.

12. (Original) The method, as recited in Claim 1, wherein after applying the charging pulse on the select one of the plurality of bit lines and before sensing the voltage difference, a voltage of the select one of the plurality of bit lines is drawn to a voltage level by a stored value in a selected memory bit cell.

13. (Previously Presented) A memory array comprising:

a plurality of bit lines;

a plurality of discharge transistors, each of the plurality of discharge transistors coupled one-to-one to a corresponding bit line of the plurality of bit lines, wherein the plurality of discharge transistors are configured to discharge the plurality of bit lines to a logic low during an inactive memory access period, wherein a selected discharge transistor of the plurality of discharge transistors is configured to stop discharging a selected bit line of the plurality of bit lines during an active memory access period;

a plurality of passgate transistors configured as a multiplexer, each of the plurality of passgate transistors coupled one-to-one to the corresponding bit line of the plurality of bit lines, the plurality of passgate transistors configured to select one of the plurality of bit lines as a sensed node; and

a pull-up transistor coupled to the sensed node, the pull-up transistor configured to provide a charging pulse to the sensed node upon entering the active memory access period.

14. (Original) The memory array, as recited in Claim 13, further comprising:

a sense amplifier coupled to the sensed node and a reference node, the sense amplifier configured to sense a difference between a voltage level on the sensed node and a voltage level on the reference node.

15. (Original) The memory array, as recited in Claim 14, wherein the difference is at least 100 millivolts.

16. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the width and the delay period are determined according to a size of the memory array.

17. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the memory array is a compilable memory and the width and the delay are calculatable according to a selectable physical size of the memory array.

18. (Original) The memory array, as recited in Claim 17, further comprising:

a pulse width selectable delay unit, wherein the pulse width selectable delay unit is configured to produce the delay period by selecting one or more units of pulse delay devices according to a mathematical equation based on the selectable size of the memory array; and

a delay period selectable delay unit, wherein the delay period selectable delay unit is configured to produce the delay period by selecting one or more units of period delay devices according to the mathematical equation.

19. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the delay period is sufficient to allow the sensed node to be pulled towards a voltage level corresponding to a stored value in a selected memory bit cell of the memory array.

20. (Original) The memory array, as recited in Claim 14, further comprising:

reference circuitry configured to generate the reference node; wherein the reference circuitry is configured to discharge the reference node low during the inactive memory access period and provide another charging pulse to the sensed node upon entering the active memory access period.

21. (Original) The memory array, as recited in Claim 13, wherein the pull-up transistor coupled to the sensed node draws a voltage of the sense node to a midpoint voltage level.

22. (Previously Presented) A circuit design tool comprising:

a compilable memory unit;

wherein a user can select a size of a memory unit to be included in a circuit design;

wherein the compilable memory unit comprises a set of instructions configured to:

calculate a delay period and a pulse width based on the size of the memory unit;

create the memory unit, wherein the memory unit comprises:

a plurality of bit lines;

a plurality of discharge transistors, each of the plurality of discharge transistors coupled to a corresponding one of the plurality of bit lines, wherein the plurality of discharge transistors are configured to discharge the plurality of bit lines to a logic low during an inactive memory access period, wherein a selected discharge transistor of the plurality of discharge transistors is configured to stop discharging a selected bit line of the plurality of bit lines during an active memory access period;

a plurality of passgate transistors configured as a multiplexer, a respective one of the plurality of passgate transistors coupled to each of the plurality of bit lines, the plurality of passgate transistors configured to select one of the plurality of bit lines as a sensed node; and

a pull-up transistor coupled to the sensed node, the pull-up transistor configured to provide a charging pulse having the pulse width to the sensed node upon entering the active memory access period.

23. (Previously Presented) The circuit design tool, as recited in Claim 22, wherein the memory unit further comprises:

a sense amplifier coupled to the sensed node, the sense amplifier configured to sense a difference between a voltage level on the sensed node and a voltage level on a reference node during the delay period after the charging pulse.

24. (Previously Presented) A circuit design tool comprising:

a compilable memory unit;

wherein a user can select a size of a memory unit to be included in a circuit design;

wherein the compilable memory unit comprises a set of instructions configured to:

calculate a delay period and a pulse width based on the size of the memory unit;

provide the memory unit;

wherein the memory unit is configured to:

discharge a plurality of bit lines during an inactive memory access period;

apply a charging pulse on a select one of the plurality of bit lines; and

sensing a voltage difference between the select one of the plurality of bit lines and a reference line;

wherein the charging pulse has a width of the pulse width and the sensing occurs during the delay period after the charging pulse.